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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,259	08/27/2001	Mario Fazio	400.058US01	4530

27073 7590 10/18/2005

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/940,259	FAZIO, MARIO	
	Examiner	Art Unit	
	Son T. Dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-86* is/are pending in the application.

4a) Of the above claim(s) *7-28 and 31-34* is/are withdrawn from consideration.

5)☒ Claim(s) *29,30,35-46,55-61,67,68 and 74-86* is/are allowed.

6)☒ Claim(s) *1,2,5,6,47,49-51,53,54,62-66 and 69-71* is/are rejected.

7)☒ Claim(s) *3,4,48,52,72 and 73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/4/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history*.

DETAILED ACTION

The Election filed on 7/14/05 has been entered.

Claims 1-86 are pending in the application.

Claims 7-28 and 31-34 are withdrawn from consideration in view of the election with traverse.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 5-6, 47, 49, 51, 53, 62-66, 69 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al (U.S. Patent No 6,128,700).

With respect to claim 1, figure 2 of Hsu et al disclose a method of operating a memory device comprising the step of communicating between a memory device (214) and a logic device (211) separated from the memory device (214), wherein the communication occurs across a local bus((the buses that connected between 211 and 214, namely ADDRESS, CONTROL, DATA). It is noted that the memory device 214 and the logic device 211 used a common power supply, then the voltage level of the local bus is compatible with the logic device.

With respect to claim 2, the system bus 204 in Hsu is isolated from the local bus (ADDRESS, DATA, CONTROL).

With respect to claim 5, the step of sending a decoded address signal is performed by the row decoder 304 in figure 3 of Hsu et al, and the step of accessing is performed by the row select 305 in figure 3 of Hsu et al.

With respect to claim 6, the step of sending a command signal is performed by the logic device 211 (figure 2, through line CONTROL), and such signal would control the operation of the memory device 214 as shown in figure 2 of Hsu.

With respect to claims 47 and 51, figure 2 of Hsu et al disclose a memory device comprising a memory array (214), at least one control signal line (CONTROL) for receiving a decoded control signal (the signal from 211 is a decode signal) from the external device (220).

With respect to claim 49 and 53, the line CONTROL is a non-buffered signal line.

With respect to claims 62, 66, figure 2 of Hsu et al discloses a memory device comprising at least one control signal line (CONTROL) for receiving controls signal line from the external device (the signal from 220 is transferred to 211 and then transferred to 214), at least one address signal line (ADDRESS) fro receiving address signal from the external device (as set forth above) and at least one data signal line (DATA) for communicating data signals between the external device (211 and 220) and the memory array 214.

With respect to claims 63-65, the address signal line, the data signal line and the control signal line of Hsu et al is substantially incapable of level translation and devoid of logic function of command interpretation and address decoding.

With respect to claim 69, figure 2 of Hsu et al disclose a memory device comprising a plurality of coupling areas on the logic device (connections at the inputs and outputs of 211), including a first portion of the plurality of coupling areas for coupling to the system bus (the connections between 211 and 220), a second portion (the ouputs of 211 that coupled to the memory 214) for coupling to the local bus (the connections between 211 and 214), a plurality of coupling areas on the memory device 214 for coupling to the local bus (the connections at the inputs of 214 to the local bus ADDRESS, DATA, CONTROL. It is noted that the connection between 211 and 214 is a direct connection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 50, 54, 70 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al in view of Wendell et al (U.S. Patent No 5,930,185).

Hsu applied as above. The difference between Hsu et al and claims 72 and 73 is that Hsu et al fail to teach the use of a wire bond and solder bump technology for connecting the logic device to the memory array. Wendell teach that the use of a wire

bond connection and solder bump connection for connecting two memory devices is well known in the art (see column 15, line 45-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hsu et al by using wire bond connections and solder bump connections for connecting two devices in order to reduce loss in a transmitting line as evidenced by Wendell.

With respect to claims 50 and 54, the use of non volatile floating gate memory cells in instead of DRAM or SRAM would have been obvious, since the method transmitting data signal, address signal and control signal between a logic device and the memory array in a non-volatile and a volatile memory cells is the same.

Allowable Subject Matter

Claims 29-30, 35-46, 55-61, 67-68, 74-86 are allowed.

Claims 3-4, 48, 52, 72-73 areobjected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to teach or disclose a nominally-buffered signal line between a logic device and a memory array, a system bus that has a bit width being less than a bit width of the local bus.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Ajanovic discloses a memory device having a system bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son T. Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on Monday to Friday 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
October 16, 2005

Son T. Dinh
Primary Examiner